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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HIEU P	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,974	CANILAO ET AL.	
	Examiner	Art Unit	
	Hieu Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/18/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-7* is/are rejected.

7)☒ Claim(s) *3,4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 7 objected to because of the following informalities:

Claim 7, line 18, "second resistor" should correctly be --third resistor--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2,6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pub. 2002/0063601) view of Kuriyama (US 6549076).

Regarding claim1, Fig. 1 of Yamamoto shows a power amplifier comprising: first and second power transistor stages receiving first and second collector supply voltages (Vc1, Vc2), respectively, the first power transistor stage comprising a first RF transistor (Q1) operating in response to the first collector supply voltage (Vc1) applied to a collector thereof and a including a base biased by a first bias voltage, the second

power transistor stage comprising a second RF transistor (Q2) operating in response to the second collector supply voltage (Vc2) applied to a collector thereof and including a base biased by a second bias voltage; and

a first stage bias circuit including first (Trb11) and second bias transistors (Trb12) and a second bias circuit including third (Trb21) and fourth bias transistors (Trb22) for providing the respective first and second bias voltages, and collectors of the first and third bias transistors operating in response to a fourth supply voltage (Vcc).

Yamamoto further discloses the bases of the first and third bias transistors being bias by a third supply voltage. But Yamamoto fails to disclose a "collectors of the second and fourth bias transistors being biased by a third supply voltage ". However, Fig. 1 of Kuriyama et al. shows (a single stage) bias circuit of a power amplifier including a first transistor (Q1) and a second transistor (Q2) being biased by a fourth (Vcont) and third (Vcc) supply voltage. If two identical stages are cascaded together, then the collectors of the first (1^{st} bias transistor from stage 1) and third (1^{st} bias transistor from stage 2) bias transistors should operate in response to a fourth supply voltage (356), and the collectors of the second (2^{nd} bias transistor from stage 1) and fourth (2^{nd} bias transistor from stage 2) bias transistors should be bias by a third supply voltage as expected for two identical stages.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Kuriyama into the circuit of Yamamoto by having "collector of the second and fourth bias transistors being biased by the third supply voltage". The ordinary artisan would have been motivated to modify

the circuit of Yamamoto in the manner set forth above for at least the purpose of obtaining high gain and efficiency for the power amplifier.

Regarding claim 2, insofar as understood, Fig. 1 of Yamamoto shows the power amplifier of claim 1 wherein the third supply voltage is independent of the first (Vc1) and second (Vc2) collector supply voltages.

Regarding claim 6, Fig. 1 of Yamamoto discloses a power amplifier comprising: first (Q1), second (Q2), third (Trb12), fourth (trb11), fifth (Trb22) and sixth (Trb21) bipolar junction transistors, each transistor including a collector, a base, and an emitter, the emitters of the first, second, third, and fifth transistors being coupled to a ground node, the collector of the fourth and sixth transistors being coupled to a bias voltage node (Vcc);

a first capacitor (Cin1) including a first terminal coupled to an input node and including a second terminal coupled to the base of the first transistor;

a second capacitor (C1) including a first terminal coupled to the collector of the first transistor (Q1) and including a second terminal coupled to the base of the second transistor (Q2);

a third capacitor (dispose at Vc1) including a first terminal coupled to the collector of the first transistor and a second terminal coupled to the ground node;

a fourth capacitor (dispose at Vc2) including a first terminal coupled to the collector of the second transistor and a second terminal coupled to the ground node;

Yamamoto fails to disclose "a first inductor including a first terminal coupled to a first supply voltage node and including a second terminal coupled to the

collector of the first transistor", "a second inductor including a first terminal coupled to a second supply voltage node and a second terminal coupled to the collector of the second transistor", "a first resistor including a first terminal coupled to a reference voltage node and including a second terminal coupled to the collector of the third transistor and the base of the fourth transistor", "a second resistor including a first terminal coupled to the reference voltage node and including a second terminal coupled to the collector of the fifth transistor and the base of the sixth transistor", "a third inductor including a first terminal coupled to the base of the third transistor and the emitter of the fourth transistor and including a second terminal coupled to the base of the first transistor" and "a fourth inductor including a first terminal coupled to the base of the fifth transistor and the emitter of the sixth transistor and including a second terminal coupled to the base of the second transistor". However, Fig. 1 of Kuriyama shows a bias circuit (for one stage) of a power amplifier including an inductor (L1) including a terminal coupled to a supply voltage node (Vc) and including a second terminal coupled to the collector of the transistor (RF1), a resistor including a first terminal coupled to a reference voltage node (Vcont) and including a second terminal coupled to the collector of the third transistor (Q1) and the base of the fourth transistor (Q2) and a inductor (L2) including a first terminal coupled to the base of the first bias transistor and the emitter of the second transistor and including a second terminal coupled to the base of the RF transistor. Again, the above circuit's elements are for one stage. There will be two or more bias circuits for two or more power transistor stages having collectors of first bias

transistor connected together and having collectors of second bias transistor connected together.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Kuriyama into the circuit of Yamamoto by having "collector of the second (2^{nd} bias transistor from first stage) and fourth (2^{nd} bias transistor from second stage) bias transistors being biased by the third supply voltage". The ordinary artisan would have been motivated to modify the circuit of Yamamoto in the manner set forth above for at least the purpose of using multi-mode bias circuit for power amplifier.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto and Kuriyama as applied to claim 1-2,6 above, and further in view of Luo et al. (US 6456163).

Regarding claim 5, Yamamoto and Kuriyama fail to disclose "the third supply voltage is coupled to the fourth supply voltage". However, Fig. of Luo shows a bias circuit in which the third supply voltage (connected to transistor 4) and the fourth supply voltage (connected to transistor 6) is coupled together.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Luo into the circuit of Yamamoto by having "the third supply voltage is coupled to the fourth supply voltage". The ordinary artisan would have been motivated to modify the circuit of Yamamoto for at least the purpose of adding stability to the system.

Claims 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (US 6549076) in view of Jarvinen (US 6052032).

Regarding claim 7, Fig. 3 of Kuriyama discloses a power amplifier comprising: first (RF1), second (Q1), and third (Q2) bipolar junction transistors, each transistor including a collector, a base, and an emitter, the emitter of the second transistor being coupled to a ground node (ground), the collector of the third transistor being coupled to a bias voltage node (Vcc);

a first inductor (L1) including a first terminal coupled to a supply voltage node (Vc) and including a second terminal coupled to the collector of the first transistor (RF1);

a first capacitor (c1) including a first terminal coupled to the first terminal of the first inductor (L1) and including a second terminal coupled to the ground node"

a second inductor (L2) including a first terminal coupled to the base of the first RF transistor and including a second terminal coupled to the base of the second transistor (Q1) and the emitter of the third transistor (Q2); and

a third resistor (R1) including a first terminal coupled to a reference voltage (Vcont) node and including a second terminal coupled to the collector of the second transistor (Q1) and the base of the third transistor (Q2).

Kuriyama fails to disclose a power amplifier having: "a first resistor including a first terminal coupled to the emitter of the first transistor and including a second terminal coupled to the ground node", " a second capacitor including a first terminal coupled to an input node and including a second terminal coupled to the second terminal of the

second inductor (306)" and "a second resistor including a first terminal coupled to the base of the first transistor and including a second terminal". However, Jarvinen [Fig. 3; col. 1, lines 33-36] discloses a power amplifier having "a first resistor (Re/m) including a first terminal coupled to the emitter of the first transistor (Q1) and including a second terminal coupled to the ground node", a second capacitor including a first terminal coupled to an input node (RF-IN) and including a second terminal coupled to the second terminal of the second inductor and "a second resistor (Rb/m) including a first terminal coupled to the base of the first transistor and including a second terminal"

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Jarvinen into the circuit of Kuriyama by having "a first resistor" or /and "a first capacitor" or/and "second resistor" in the circuit. The ordinary artisan would have been motivated to modify the circuit of Yamamoto in the manner set forth above the purpose of adding stability to the transistor (by adding first resistor), or blocking interference from supply voltage (by using the first capacitor) or matching impedance as well as setting current (by using the second resistor).

Allowable Subject Matter

Claim 3,4 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 3, the prior art of record fails to disclose or suggest a structure of a power amplifier comprising "a first housing including first, second, third and fourth terminals, the first terminal being coupled to receive the first collector supply voltage, the second terminal being coupled to receive the second collector supply voltage, the third and fourth terminals being coupled to receive the third and fourth supply voltages, respectively" in combination with the rest of the limitations of the claim(s).

Regarding claim 4, the prior art of record fails to disclose or suggest a power amplifier comprising "a second housing of a power amplifier that includes fifth, sixth, seventh and eight terminals disposed on the second housing in a manner similar to the first, second, third and fourth terminals of the first housing, the fifth and sixth terminals coupled to receive fifth and sixth supply voltages, respectively, the seventh terminal coupled to receive an RF signal, the eighth terminal coupled to receive a seventh supply voltage" in combination with the rest of the limitations of the claim(s)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional references (see PTO-892) show further analogous prior art circuitry

These arts are deemed relevant and should be carefully reviews before any amendment is filed

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number 571-272-0218. The examiner can normally be reached on 8:00 AM – 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hn

Zandra V Smith
Primary Examiner
7/25/09